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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,270	02/20/2004	Mark Bilak	FIS920040015US1	2269

32074 7590 07/01/2008

INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 300-482
2070 ROUTE 52
HOPEWELL JUNCTION, NY 12533

EXAMINER	
CONNOLLY, MARK A	

ART UNIT	PAPER NUMBER
2115	

MAIL DATE	DELIVERY MODE
07/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/708,270	BILAK, MARK	
	Examiner	Art Unit	
	MARK CONNOLLY	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *17-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 and 25 have been presented for examination.

2. Applicant's arguments with respect to claims 1-16 and 25 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-10, 12, 15-16 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujioka[1] in view of Halepete[2] in view of Justice[3].

5. Referring to claim 1, Fujioka teaches the apparatus for adaptively controlling power consumption within an electronic system substantially comprising:

a. an integrated circuit adapted to transmit voltage control information corresponding to a minimum operating voltage [fig. 1, abstract and 0051].

b. a storage element coupled to said integrated circuit, adapted to store a minimum operating voltage [fig. 1, abstract and 0048].

c. a variable voltage regulator coupled to said integrated circuit, adapted to receive said voltage control information from said integrated circuit, and supply an operating voltage to said integrated circuit in response to and representative of said voltage control information [abstract, 0037 and 0051].

d. a communication link coupled to said integrated circuit and said variable voltage regulator, adapted to link said integrated circuit to said variable voltage regulator so that

[1] As cited in the previous Office Action.

said integrated circuit may transmit said voltage control information to said variable voltage regulator [0048].

In summary, Fujioka teaches a system which stores voltage control information in memory 206 and uses that information to set an operating voltage if it is determined that the operable voltage is an operable minimum voltage.

Although Fujioka teaches transmitting voltage control information, the voltage control information corresponds to a minimum operating voltage uniquely determined for the integrated circuit which is different than the predetermined nominal voltage for a family of the integrated circuits [0044] and not the *difference between* a minimum operating voltage uniquely determined for the integrated circuit and the predetermined nominal voltage selected for a family of integrated circuits. Halepete teaches that when decreasing voltage it can be performed in either a single step (as is taught in Fujioka) or in a series of incremental steps [col. 7 lines 33-35]. It would have been obvious to one of ordinary skill in the art to try decreasing the voltage to a minimum operating voltage in a series of steps rather than in a single step because a person with ordinary skill has good reason to pursue the known options within his or her technical grasp. Because the voltage is controlled by transmitting voltage control information corresponding to the voltage to be immediately output by the voltage regulator, it is interpreted that when decreasing the voltage in a plurality of steps that the voltage control information would represent the difference in voltage between a current voltage level (including the initial predetermined voltage for the family of integrated circuits) and the next voltage level to be stepped down to until the minimum operating voltage is reached.

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[2] As cited in the previous Office Action.

Although the Fujioka-Halepete teaches transmitting voltage control information corresponding to a difference between a minimum operating voltage uniquely determined for the integrated circuit and a predetermined nominal voltage selected for a family of circuits, it is not explicitly taught that the voltage control information further comprises guard band. Justice teaches using guard band during device testing [page 1]. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the use of guard band into the voltage control information because when testing limits in a device under test, measurements must be made which can introduce inaccuracies. By including guard band, it would allow the system to compensate for any inaccuracies introduced by the measurement devices as taught by Justice [page 1].

6. Referring to claim 2, Fujioka teaches the voltage control information is determined during external testing of the IC [abstract].

7. Referring to claim 3, Fujioka teaches the storage element being a non-volatile memory [0073].

8. Referring to claim 4, Fujioka teaches a temperature sensor for measuring the temperature of the integrated circuit [0037].

9. Referring to claim 5, Fujioka teaches modifying voltage control information in response to temperature data [0011].

10. Referring to claim 6, Fujioka teaches a built-in-self-test to determine the minimum operating voltage [abstract and 0055].

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[3] As cited in a previous Office Action.

11. Referring to claim 7, Fujioka teaches a temperature sensor for measuring the temperature of the integrated circuit [0037].

12. Referring to claim 8, Fujioka teaches modifying voltage control information in response to temperature data [0011].

13. Referring to claims 9-10 and 12, these are rejected on the same basis as set forth hereinabove. Fujioka teaches the apparatus and therefore teaches the method performed by the apparatus.

14. Referring to claim 13, Fujioka teaches adjusting a voltage to an integrated circuit and testing with the lowered voltage in order to determine an effective minimum voltage to be applied to the integrated circuit [0062-0063].

15. Referring to claims 15-16, these are rejected on the same basis as set forth hereinabove. Fujioka teaches the apparatus and therefore teaches the method performed by the apparatus.

16. Referring to claim 25, this is rejected on the same basis as set forth hereinabove.

17. Claims 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujioka, Halepete and Justice as applied to claims 1-10, 12-13, 15-16 and 25 above, and further in view of DeLuca[4].

18. Referring to claim 11, although Fujioka teaches performing a test to determine a minimum operating voltage, it is not explicitly taught that the voltage is determined by testing timing critical paths of the integrated circuit. In particular, Fujioka does not teach that voltage is determined based on the speed of the integrated circuit. DeLuca teaches determining a minimum

[4] As cited in the previous Office Action.

operating voltage of an integrated circuit based on a required speed [col. 2 lines 26-31 and col. 3 lines 16-17]. It would have been obvious to one of ordinary skill in the art at the time of the invention to include a means to select an appropriate minimum voltage based on speed because DeLuca explicitly teaches that under certain activities, certain speeds are required in order for the integrated circuit to operate normally.

19. Referring to claim 14, this is rejected on the same basis as set forth hereinabove.

Response to Arguments

20. Applicant's arguments filed 4/18/08 have been fully considered but they are not persuasive.

21. In the REMARKS, applicant argues in substance that "although Justice teaches 'guard bands' generally, Applicant believes Justice either alone or in combination with the other cited references, does not teach introducing the guard band to a 'minimum operating voltage uniquely determined for the integrated circuit.'"

22. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

In addition, the Fujioka-Halepete system teaches testing to determine a difference between a minimum operating voltage and a predetermined nominal voltage for an IC as shown above. Because the voltage difference is determined through testing, it is prone to measurement inaccuracies as suggested by Justice. Therefore, to remedy for these inaccuracies Justice teaches introducing guard band because it provides a means to offset any of the measurement inaccuracies inherent to the testing process.

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MARK CONNOLLY whose telephone number is (571)272-3666. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Mark Connolly/
Primary Examiner, Art Unit 2115
6/27/08

Mark Connolly
Primary Examiner
Art Unit 2115